IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	**10/763,670**	Examiner:	**Tim T. Vo**
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Filed:	**01/24/2004**	Art Unit:	**2112**
Title:	**Console Chip And One-Bus System**		

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/Jason Z. Lin/
Signature

Commissioner for Patents
P.O. Box 1450
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Sir:

AMENDMENT A

In response to the Office Action mailed **02/13/2006**, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Abstract begin on page 7 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 8 of this paper.

Remarks begin on page 11 of this paper.

AMENDMENTS TO THE SPECIFICATION:

Page 1, amend Title as:

CONSOLE CHIP AND ~~ONE-BUS~~ SINGLE MEMORY BUS SYSTEM

Page 1, amend paragraph [0003] as:

[0003] FIG. 1 shows a conventional two-bus system, including a CPU/Sound/Graphic unit [[1]] 11, a program and sound memory [[2]] 12, a graphic memory [[3]] 13, a TV/LCD signal unit [[4]] 14, a program and sound bus [[5]] 15, and a graphic bus [[6]] 16. CPU/Sound/Graphic unit [[1]] 11 communicates with program and sound memory [[2]] 12 through program and sound bus [[5]] 15, while with graphic memory [[3]] 13 through graphic memory [[6]] 16. After ~~processed or~~ processing, the displayed data are then sent to TV/LCD signal unit [[4]] 14, and separated into video output, and audio outputs.

Page 2, amend paragraph [0004] as:

[0004] Conventional structure of two-bus multi-media computer systems [[have]] has several shortcomings due to having two buses. As the CPU/Sound/Graphic unit [[1]] 11 can only communicate with a memory at one time, the two buses must be synchronized in communicating with CPU/Sound/Graphic unit [[1]] 11. The synchronization adds extra overhead to CPU/Sound Graphic unit [[1]] 11 and wastes precious processing cycles. Further more, the circuit complexity of CPU/Sound/Graphic unit 11 increases ~~1 increase~~ because it also [[need]] needs extra circuit to perform the synchronization.

Page 2, amend paragraph [0005] as:

[0005] The object of the present invention is to provide a ~~one-bus~~ computer system with a single memory bus so that the CPU performance can be improved by avoid wasting precious CPU cycles on bus synchronization, and waiting for [[slow]] memory with lower speed.

Page 2, amend paragraph [0006] as:

[0006] Another object of the present invention is to provide a ~~one-bus~~ computer system with a single memory bus so that the circuit complexity of CPU can be reduced due to the elimination of bus synchronization task, which, in turn, ~~will reduce~~ reduces the number of the pins ~~pin number~~ required.

Page 3, amend paragraph [0011] as:

[0011] FIG. 2 shows a schematic view of a ~~one-bus~~ single memory bus computer system for the present invention.

Page 3, amend paragraph [0012] as:

[0012] FIG. 3 shows a detailed block diagram of a ~~one-bus~~ single memory bus computer system of the present invention.

Page 4, amend paragraph [0015] as:

[0015] As shown in FIG. 2, the present invention of a ~~one-bus~~ single memory bus multi-media computer system comprises a CPU/Sound/Graphic unit 21 connected to a program and sound bus 25 and a graphic bus 26, a bus arbitrator 22 connected to program and sound bus 25 and graphic bus 26 on one side, and ~~one-bus~~ single memory bus 27 on

the other side, a program and sound and graphic memory 23 connected to ~~one bus~~ single memory bus 27, and a TV/LCD signal unit 24 for outputting audio and video signals. CPU/Sound/Graphic unit 21 requests [[said]] the program and sound and graphic memory 23 by memory addresses, processes data returned from program and sound and graphic memory 23, and sends the signals to TV/LCD signal unit 24 for outputting. Bus arbitrator 22 sits between CPU/Sound/Graphic 21 and program and sound and graphic memory 23 to arbitrate the memory requests from CPU/Sound/Graphic unit 21 to program and sound and graphic memory 23. Program and sound memory 12 and graphic memory 13 of FIG. 1 are consolidated into a program and sound and graphic memory 23, which communicates with CPU/Sound/Graphic unit 21 through a bus arbitrator 22 with a single memory bus 27. The addition of bus-arbitrator 22 can relieve CPU/Sound/Graphic unit 21 from performing bus synchronization and waiting for the slow memory to catch up.

Pages 4-5, amend paragraph [0016] as:

[0016] FIG. 3 shows a detailed block diagram of a computer system of the present invention. As shown in FIG. 3, the system includes a CPU 32, a sound unit 33, a graphic unit 34, and internal program memory 31, an internal video memory 35, a bus-arbitrator 22, and an external memory 37. Internal program memory 31 receives a memory request address from address bus 31a and exchanges the data for that memory address with CPU 32 through data bus 31b. CPU 32 also sends CPU address ports information 32a to sound unit 33, and relays [[PCU]] CPU address ports information 33a to graphic unit 34. All CPU 32, sound unit 33, and graphic unit 34 send memory request addresses to bus

arbitrator 22 through address buses 32b, 33b, and 34c, respectively. The data are exchanged from and to bus arbitrator 22 through data buses 32c, 33c, and 34d, respectively. An additional address bus 34a and data bus 34b are used by graphic unit 34 to communicate with internal video memory 35. Bus arbitrator 22 communicates with an external memory 37 through an address bus 36a and a data bus 36b. The ~~output~~ outputs from sound unit 33 are audio1 and audio2 streams, and graphic unit 34 outputs video stream.

Page 5, amend paragraph [0017] as:

[0017] Basically, bus arbitrator 22 arbitrates the bus accessibility with the rule that a memory request to a faster memory is given a higher priority to access the bus without the pre-emptive capability. Hence, when the bus is available and two or more memories request to use the bus, the request to the memory having the fastest speed is given the highest priority, and the others will wait [[unit]] <u>for</u> their respective turn to access the memory. On the other hand, when the bus is unavailable and two or more memories request to use the bus, all the requests for the bus accessing are given a priority based on their memory speed, and wait [[unit]] <u>for</u> their respective turn. The memory currently accessing the bus will finish the use of bus regardless of its memory speed.

Pages 5-6, amend paragraph [0018] as:

[0018] FIG. 4 shows a block diagram of the sound unit of the system of the present invention. As shown in FIG. 4, the sound unit includes four rhythm channels 42, 43, 44, 45, two low frequency channels 46, 47, two noise channels 48, 49, a built-in DM 50, and a built-in PCM 51. CPU address ports 41 provide signals for controlling the operation of

the sound unit. The sound unit also includes two independent outputs that are a first audio and a second audio.

Page 6, amend paragraph [0019] as:

[0019] FIG. 5 shows a block diagram of the bus arbitrator of the present invention. As shown in FIG. 5, the bus arbitrator includes an address bus multiplexer 61 and a first data register 62. Address bus multiplexer 61 takes two inputs, a first bus address 61a and a second bus address 61b, and multiplex to generate an output, one-bus ~~address61c~~ address 61c. In the embodiment, the first bus 61a is a low frequency program and sound system bus, and the second bus 61b is a high frequency video bus. The data from one-bus, called one-bus data 62c, can be either temporarily stored in the first data register 62 or directly outputted to a second data bus. The operation of address bus multiplexer 61 and the first data register 62 is controlled by a bus control signal, second bus signal OEB. When the second bus signal OEB is low, the address bus multiplexer takes the second bus address 61b and outputs one-bus ~~address61c~~ address 61c. At the same time, the first data register 62 stores the one-bus data 62c and outputs a first bus data 62a. On the other hand, when the second bus signal OEB is high, it is the accessing cycle for the first bus untill the second bus signal OEB becomes low. During the accessing cycle of the first bus, one-bus data is transported to the first bus data. The video system gets a second bus data 62b before the second bus signal OEB transits from low to high.

AMENDMENTS TO THE ABSTRACT:

A ~~one-bus~~ single memory bus multi-media computer system is provided, including a CPU/Sound/Graphic unit, a bus arbitrator, a program and sound and graphic memory for communicating with the CPU/Sound/Graphic unit and the bus arbitrator. Only a single memory bus is required as communication ~~communications~~ is through the bus arbitrator. The addition of the bus-arbitrator can relieve the CPU/Sound/Graphic unit from performing bus synchronization and waiting for the slow memory to catch up.

AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A ~~one-bus~~ single memory bus multi-media computer system, comprising:

a CPU/Sound/Graphic unit connected to a program and sound bus and a graphic bus;

a bus arbitrator connected to said program and sound bus and said graphic bus on ~~one~~ a first side, and ~~said one-bus on the other~~ a single memory bus on a second side, said bus arbitrator including an address bus multiplexer for receiving a program and sound bus address and a graphic bus address as inputs, and outputting a single memory bus address, and a first data register for storing memory data from said single memory bus, said memory data being controlled by a bus control signal OEB for being temporarily stored in said first data register or directly outputted to a graphics data bus;

a program and sound and graphic memory connected to said ~~one-bus~~ single memory bus; and

a TV/LCD signal unit for outputting audio and video signals;

wherein said CPU/Sound/Graphic unit requests said program and sound and graphic memory by memory addresses, processes data returned from said program and sound and graphic memory, and sends [[the]] signals to said TV/LCD signal unit for outputting, said bus arbitrator sits between said CPU/Sound/Graphic and said program and sound and graphic memory to arbitrate [[said]] the memory requests from said CPU/Sound/Graphic unit to said program and sound and graphic memory.

2. (Currently Amended) The system as claimed in claim 1, wherein said ~~one-bus~~ single memory bus further comprises an address bus for sending address and a data bus for

sending data.

3. (Original) The system as claimed in claim 1, wherein said program and sound bus further comprises an address bus for sending address and a data bus for sending data.

4. (Original) The system as claimed in claim 1, wherein said graphic bus further comprises an address bus for sending address and a data bus for sending data.

5. (Currently Amended) The system as claimed in claim 1, wherein said bus arbitrator uses [[the]] a rule that a memory request to a faster memory is given a higher priority to access ~~the~~ said single memory bus without [[the]] pre-emptive capability.

6-7. (Cancelled).

8. (Currently Amended) The system as claimed in claim [[6]] 1, wherein said ~~second~~ bus control signal OEB controls the operation of said address multiplexer and said first data register with the following rules:

(a) when said ~~second~~ bus control signal OEB is low, said address bus multiplexer takes said graphics ~~second~~ bus address ~~and outputs one bus~~ for outputing said single memory bus address, at the same time, said first data bus register stores said ~~one bus~~ single memory bus data and outputs said [[first]] program and sound bus data;

(b) when said ~~second~~ bus control signal OEB is high, it is the accessing cycle for said [[first]] program and sound bus untill said ~~second~~ bus control signal OEB becomes low, during the accessing cycle of said [[first]] program and sound bus, ~~one bus~~ said single memory bus data is transported to said [[first]] program and sound bus data; and

(c) said ~~second~~ graphics bus gets said ~~second~~ graphics bus data before said ~~second~~

bus control signal OEB transits from low to high.

9. (Currently Amended) A system chip for processing audio and video data, comprising:

a CPU/Sound/Graphic unit connected to a program and sound bus and a graphic bus;

a bus arbitrator connected to said program and sound bus and said graphic bus on ~~one~~ a first side, and ~~said one bus on the other~~ a single memory bus on a second side, said bus arbitrator including an address bus multiplexer for receiving a program and sound bus address and a graphic bus address as inputs, and outputting a single memory bus address, and a first data register for storing memory data from said single memory bus, said memory data being controlled by a bus control signal OEB for being temporarily stored in said first data register or directly outputted to a graphics data bus;

a program and sound and graphic memory connected to said ~~one-bus~~ single memory bus; and

a TV/LCD signal unit for outputting audio and video signals;

wherein said CPU/Sound/Graphic unit requests said program and sound and graphic memory by memory addresses, processes data returned from said program and sound and graphic memory, and sends [[the]] signals to said TV/LCD signal unit for outputting, said bus arbitrator sits between said CPU/Sound/Graphic and said program and sound and graphic memory to arbitrate [[said]] the memory requests from said CPU/Sound/Graphic unit to said program and sound and graphic memory.

REMARKS

In the Office Action, claims 1-8 are rejected under 35 U.S.C. §112 as being indefinite because of the preamble "one-bus multimedia computer system", claims 1-5 and 9 are rejected under 35 U.S.C. §102(b) as being anticipated by Ishida, and claim 6-8 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response to the office action, the term "one-bus" is replaced with "single memory bus" throughout the title, specification and claims to clearly describe the subject matter of the invention and to overcome the indefiniteness pointed out by the examiner.

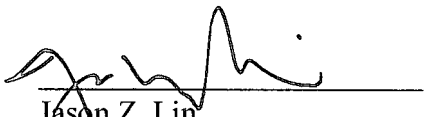
Claim 1 is now amended to include the limitations of the allowable matter of claim 6 which is canceled. The amended claim 1 is allowable. A few informalities are corrected in claims 2, 5 and 8. By virtue of dependency claims 2-5 and 8 should also be allowable. Similarly, claim 9 is amended to include the limitations of the allowable matter of claim 6 so as to render claim 9 allowable.

Claims 6-7 are cancelled.

The above amendment has been made without prejudice. Claims 1-5 and 8-9 are now in full condition for allowance. The specification has been amended to correct a few

editorial and grammatical errors. Applicant respectfully requests that a timely Notice of Allowance be issued for this application.

Respectfully submitted,



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